AMENDMENTS TO THE CLAIMS

Claims 1-15 and 24-27 were pending in the Application. Claim 1 is an independent claim and claims 2-9 depend therefrom. Claim 10 is an independent claim and claims 11-12 depend therefrom. Claim 13 is an independent claim and claims 14-15 depend therefrom. Claim 24 is an independent claim and claims 25-27 depend therefrom. Claims 16-23 and 28-40 were previously canceled. Claims 1, 10, 12 and 25-26 are currently amended. Claim 11 is currently canceled.

Listing of Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising:

a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage,

wherein the first state comprises at least a portion of a memory address of the first memory block irrespective of a position of the first logic circuit.

2. (Original) The memory management circuit of claim 1, further comprising a second logic circuit associated with a first memory segment of the first memory block, the second logic circuit having a first state when the first memory segment is available for data storage and a second

state when the first memory segment is not available for data storage.

3. (Previously Presented) The memory management circuit of claim 1, wherein the second state is a state of a single logic bit.

4. (Previously Presented) The memory management circuit of claim 1, wherein the second state comprises information of an offset to a next available memory block or memory segment.

5. (Original) The memory management circuit of claim 1, further comprising a second logic circuit having a plurality of logic sub-circuits, each logic sub-circuit corresponding to a respective one of the memory segments of the first memory block, each logic sub-circuit having a first state when its respective memory segment is available for data storage and a second state when its respective memory segment is not available for data storage.

6. (Previously Presented) The memory management circuit of claim 2, wherein the first state of the second logic circuit comprises at least a portion of a memory address of the first memory segment.

7. (Original) The memor y management circuit of claim 2, further comprising a third logic circuit that converts the first state of the first logic circuit and the first state of the second logic circuit to the memory address of the first memory segment.

8. (Previously Presented) The memory management circuit of claim 2, wherein the first and

second states of the first logic circuit are states of a plurality of logic bits, and the first and second states of the second logic circuit are states of a plurality of logic bits.

9. (Previously Presented) The memory management circuit of claim 2, wherein the first state of the second logic circuit is indicative of a memory offset between the memory address of the first memory block and the memory address of the first memory segment.

10. (Previously Presented) A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management circuit comprising:

a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage; and

a second logic circuit having a first state when a first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for data storage;

wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to the first state of the second logic circuit.

11. (Canceled)

12. (Currently Amended) The memory management circuit of claim 10 ~~11~~, wherein the first and second states of the second logic circuit are single-bit logic states.

13. (Previously Presented) A memory management circuit for managing a memory having a plurality of memory blocks, each memory block having a plurality of memory segments, the memory management system comprising:

a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when any of the memory segments of the first memory block are available for data storage and a second state when none of the memory segments of the first memory block are available for storage;

wherein the second state of the first logic circuit comprises information indicating an offset to available memory.

14. (Previously Presented) The memory management circuit of claim 13, further comprising a second logic circuit having a first state when a first memory segment of the first memory block is available for data storage and a second state when the first memory segment of the first memory block is not available for storage.

15. (Previously Presented) The memory management system of claim 14, wherein the second state of the second logic circuit comprises information indicating an offset to an available memory segment.

16-23. (Canceled)

24. (Previously Presented) A method for managing memory, the method comprising:

analyzing a state of a first logic circuit to determine whether a block of memory segments includes a memory segment that is available for data storage, the first logic circuit having a

first state when the block of memory segments has a memory segment that is available for data storage and a second state when the block of memory segments does not have a memory segment that is available for data storage; and

if the block of memory segments includes a memory segment that is available for data storage, identifying a memory segment in the block of memory segments that is available for data storage.

25. (Currently Amended) The method of claim 24, wherein the first state comprises at least a portion of a memory address of the block of memory segments irrespective of a position of the first logic circuit.

26. (Currently Amended) The method of claim 24, wherein:

each of the memory segments is associated with a respective second logic circuit having a first state when the memory segment of the block of memory segments is available for data storage and a second state when the memory segment of the block of memory segments is not available for data storage; and

the first state of the first logic circuit comprises a number of available memory segments in the block of memory segments, said number of available memory segments corresponding to the first state of each of the respective second logic circuits.

27. (Previously Presented) The method of claim 26, wherein the second state comprises information indicating an offset to available memory.

28-40. (Canceled)